AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. –14. (canceled)

15. (new) A method of forming a semiconductor device, comprising the steps of:

forming at least one first transistor and at least one second transistor in an insulating layer on a semiconductor substrate, wherein the first transistor comprises a first gate and a first gate dielectric layer, and the second transistor comprises a dummy gate structure;

removing the dummy gate structure to form an opening exposing the semiconductor substrate;

forming a conformal second gate dielectric layer on interior and bottom surfaces of the opening; and

forming a second gate on the second gate dielectric layer to fill the opening.

16. (new) The method of claim 15, wherein the dummy gate structure comprises a dummy polysilicon gate.

17. (new) The method of claim 15, wherein the first gate is a polysilicon gate.

18. (new) The method of claim 17, further comprising forming a salicide layer on a top surface of the polysilicon gate.

19. (new) The method of claim 15, wherein the second gate is a metal gate.

20. (new) The method of claim 19, wherein the metal gate comprises titanium, tungsten, copper or aluminum.

21. (new) The method of claim 15, wherein the first dielectric layer is thicker than the second dielectric layer.

22. (new) The method of claim 15, wherein a thickness of the first dielectric layer is about between 300Å and 600Å.

23. (new) The method of claim 15, wherein a thickness of the second dielectric layer is about between 50Å and 150Å.

24. (new) The method of claim 15, wherein spacers are formed between the dummy gate structure and the insulating layer.

25. (new) The method of claim 15, wherein the second dielectric layer is a high-k dielectric layer comprising silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), oxide-nitride-oxide (ONO), silicon oxide (Si_2O), tantalum pentoxide (TaO_5), titanium oxide (TiO_2), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_5), barium titanium oxide ($BaTiO_3$) or strontium titanium oxide ($SrTiO_3$).

26. (new) An integrated process of forming a high-voltage transistor and a low-voltage transistor, comprising the steps of:

forming at least one first transistor and at least one second transistor in an insulating layer on a semiconductor substrate, wherein the first transistor comprises a high-voltage gate and a first gate dielectric layer, and the second transistor comprises a dummy gate structure;

removing the dummy gate structure to form an opening exposing the semiconductor substrate;

forming a conformal second gate dielectric layer on interior and bottom surfaces of the opening; and

forming a low-voltage gate on the second gate dielectric layer to fill the opening.

27. (new) The integrated process of claim 26, wherein the dummy gate structure comprises a dummy polysilicon gate.

28. (new) The integrated process of claim 26, wherein the high-voltage gate is a polysilicon gate.

29. (new) The integrated process of claim 28, further comprising forming a salicide layer on a top surface of the polysilicon gate.

30. (new) The integrated process of claim 26, wherein the low-voltage gate is a metal gate.

31. (new) The integrated process of claim 30, wherein the metal gate comprises titanium, tungsten, copper or aluminum.

32. (new) The integrated process of claim 26, wherein the first dielectric layer is thicker than the second dielectric layer.

33. (new) The integrated process of claim 26, wherein a thickness of the first dielectric layer is about between 300Å and 600Å.

34. (new) The integrated process of claim 26, wherein a thickness of the second dielectric layer is about between 50Å and 150Å.

35. (new) The integrated process of claim 26, wherein spacers are formed between the dummy gate structure and the insulating layer.

36. (new) The integrated process of claim 26, wherein the second dielectric layer is a high-k dielectric layer comprising silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), oxide-nitride-oxide (ONO), silicon oxide (Si_2O), tantalum pentoxide (TaO_5), titanium oxide (TiO_2), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_5), barium titanium oxide ($BaTiO_3$) or strontium titanium oxide ($SrTiO_3$).